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| ELEC 402 |
| Project 2 Report |
| Synthesized Version of Project 1; https://github.com/mchuahua/ELEC402/tree/master/Proj2 |

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**Mapped Verilog generated by RTL Compiler**

See ./fsm\_map.v (or appendix A)

**Visual Waveforms showing state transitions from mapped Verilog:**

As the synthesized mapped Verilog doesn’t contain enum from the Proj1 testbench, it was decided that in order to verify the state transitions, the simplest method would be to utilize a visual comparison between the Proj1 waveforms and Proj2 waveforms. This was also the easiest method to confirm the state transitions, as the output/input signals of the DUT depend on the states and state transitions. Therefore, although assertions were not used in the Proj2 tb, just by having the waveforms match (disregarding delay) means that the state transitions also match, and work correctly.

Below is the waveform for the mapped Verilog (first):

Timeline

Description automatically generated

And below is the Proj1 waveform with verifiable states:

A picture containing diagram

Description automatically generated

There are various signals to note that will be listed below. One major point is that the Ready signal is asserted when state is in IDLE. The test\_num signal can also allow the user to glean information about what is happening. To explain why this is possible:

1. Test num 0 is in IDLE. Ready is asserted. This is correct.
2. Test num 1 sees that ready is asserted and deasserted, as it transitions back and forth due to invalid PIN (0-9). This is correct.
3. Test num 2 sees that after a valid PIN, state should not be in IDLE. This is correct. If it wasn’t the ready signal should be asserted just as in test\_num 1.
4. Test num 3 sees that withdrawal (0) makes FSM go to the correct state. Seeing that ready isn’t asserted, the state is not in IDLE and is proceeding along.
5. Test num 4 sees that reset works and if deposit (1) goes to correct state. Notice that the two waveforms are the same (albeit Proj2 waveform has delay). Therefore the deposit states are correctly being transitioned to.
6. Test num 5 checks to see if deposited correct. Notice the open atm output is being correctly triggered in the proj 2 waveform, matching the proj 1 waveform.
7. Test num 6 checks to see if reset + withdrawal was correct. Again, both waveforms match. At the end of test num 6, we see the open\_atm\_dispense was triggered properly, just as in proj 1 waveform. This suggests that the withdrawal states are correctly being transitioned to.
8. The next three tests can be understood by understanding the state functionality. The state for looping an amount check is before the state for looping the withdraw card check, which then goes to IDLE if card is withdrawn. Notice in test num 7 the input amount is changed. This should trigger a loop, as there are insufficient funds. This matches proj1 waveform. Now, if we change the input amount back to 1, the state should continue along and wait for the bank card to be withdrawn. In test num 8, the card is never withdrawn, and our waveforms match. Likewise, the bank card is then withdrawn, and in test num 9 we see Ready being asserted, indicating that we are indeed in IDLE.

**Report from RTL Compiler showing total number of cells in project**

See ./fsm\_area.rpt

Text

Description automatically generated

Seems as expected; passing above minimum threshold requirement of 100 cells. Expected to be relatively larger than 100 cells because FSM was slightly above trivial (10+ states, various state transitions), as well as the amount of logic statements used (regs/wires).

See ./fsm\_timing.rpt

A picture containing graphical user interface

Description automatically generated

Timing slack is positive, which is good. Initial following according to the tutorial document gave a timing slack of 1ps, but after following Sean’s advice on piazza on how to change the timing unit, the slack increased. This is good because it allows more leeway for signals to propagate.

See ./fsm\_gates.rpt

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This is expected and matches expectations. NAND and NOR should be the highest because they are considered as universal gates and are easier and more economical to fabricate. There is more logic instances than sequential or inverter because Cadence is able to optimize some of the unused sequential logic to logic constants (LUTs). This effectively reduces power (for propagating unnecessary buses) and reduces size of area that might otherwise be used. Additionally, the AOI (AND-OR-Invert) gates are used as complex gates can be more efficiently built than discrete representations, as the discrete representation is usually more expensive in cost and slower in propagation time from input to output.

**Changed Designs from Project 1**

For testbench, all assertions were commented out. This can be seen in fsm\_tb.sv.

For fsm, 2 small changes were made:

Text

Description automatically generated with medium confidence

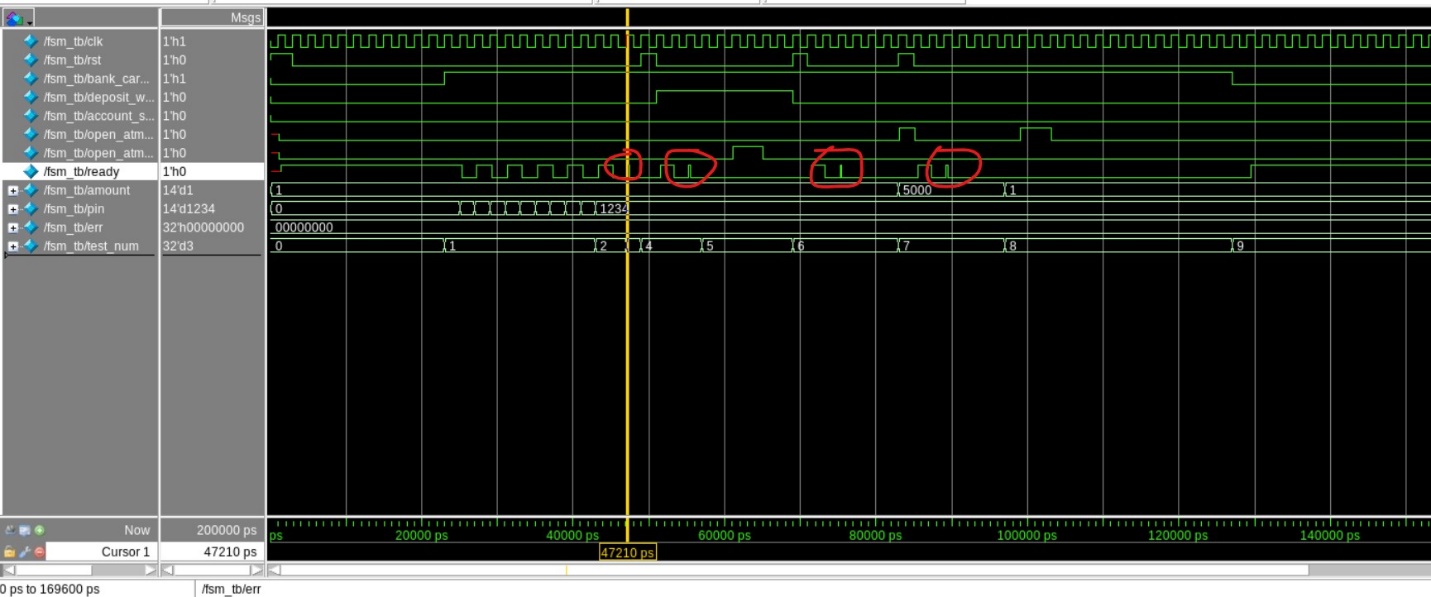
1. Last three coloured lines were fixes to allow the system Verilog to be able to be synthesized. Blocking assignments were incorrectly used (typo) instead of non-blocking, as it is a sequential logic block rather than combinational.
2. First three coloured lines switched to allow correct functionality in waveform. See below:

Working with fixes mentioned above:

Timeline

Description automatically generated

Not working without fixes:



Without the fixes, as indicated by the red circles there were some unintended assertions of the ready signal. From intuition and clarifying with the TA, it turns out that using the “==” produces a longer enough propagation time (cascading transistor delay) in comparison to “!=” such that the states are not propagating fast enough for the state machine to function correctly. And as such the bits that correspond to the correct state are not being flipped fast enough, causing this spike as ready is being incorrectly asserted.

Alternatively, this could also suggest that rather than changing the code, the clock period may also be increased, although this has not been attempted as the fix has worked.

**Appendix A – fsm\_map.v code**

// Generated by Cadence Encounter(R) RTL Compiler RC14.13 - v14.10-s027\_1

// Verification Directory fv/fsm

module fsm(clk, rst, bank\_card\_insert, deposit\_withdrawal\_selection,

account\_selection, amount, pin, open\_atm\_dispense,

open\_atm\_receive, ready);

input clk, rst, bank\_card\_insert, deposit\_withdrawal\_selection,

account\_selection;

input [13:0] amount, pin;

output open\_atm\_dispense, open\_atm\_receive, ready;

wire clk, rst, bank\_card\_insert, deposit\_withdrawal\_selection,

account\_selection;

wire [13:0] amount, pin;

wire open\_atm\_dispense, open\_atm\_receive, ready;

wire [13:0] savings\_local;

wire [13:0] chequing\_local;

wire [31:0] state;

wire n\_0, n\_1, n\_2, n\_3, n\_4, n\_5, n\_6, n\_7;

wire n\_8, n\_9, n\_10, n\_11, n\_12, n\_13, n\_14, n\_15;

wire n\_16, n\_17, n\_18, n\_19, n\_20, n\_21, n\_22, n\_23;

wire n\_24, n\_25, n\_26, n\_27, n\_28, n\_29, n\_30, n\_31;

wire n\_32, n\_33, n\_34, n\_35, n\_36, n\_37, n\_38, n\_39;

wire n\_40, n\_41, n\_42, n\_43, n\_44, n\_45, n\_46, n\_47;

wire n\_48, n\_49, n\_50, n\_51, n\_52, n\_53, n\_54, n\_55;

wire n\_56, n\_57, n\_58, n\_59, n\_60, n\_61, n\_62, n\_63;

wire n\_64, n\_65, n\_66, n\_67, n\_68, n\_69, n\_70, n\_71;

wire n\_72, n\_73, n\_74, n\_75, n\_76, n\_77, n\_78, n\_79;

wire n\_80, n\_81, n\_82, n\_83, n\_84, n\_85, n\_86, n\_87;

wire n\_88, n\_89, n\_90, n\_91, n\_92, n\_93, n\_94, n\_95;

wire n\_96, n\_97, n\_98, n\_99, n\_100, n\_101, n\_102, n\_103;

wire n\_104, n\_105, n\_106, n\_107, n\_108, n\_109, n\_110, n\_111;

wire n\_112, n\_113, n\_114, n\_115, n\_116, n\_117, n\_118, n\_119;

wire n\_120, n\_121, n\_122, n\_123, n\_124, n\_125, n\_126, n\_127;

wire n\_128, n\_129, n\_130, n\_132, n\_133, n\_134, n\_135, n\_136;

wire n\_137, n\_138, n\_139, n\_140, n\_141, n\_142, n\_143, n\_144;

wire n\_145, n\_146, n\_147, n\_148, n\_149, n\_150, n\_151, n\_152;

wire n\_153, n\_154, n\_155, n\_156, n\_157, n\_158, n\_159, n\_160;

wire n\_161, n\_162, n\_163, n\_164, n\_165, n\_166, n\_167, n\_168;

wire n\_169, n\_170, n\_171, n\_172, n\_173, n\_174, n\_175, n\_176;

wire n\_177, n\_178, n\_179, n\_180, n\_181, n\_182, n\_183, n\_184;

wire n\_185, n\_186, n\_187, n\_188, n\_189, n\_190, n\_191, n\_192;

wire n\_193, n\_194, n\_195, n\_196, n\_197, n\_198, n\_199, n\_200;

wire n\_201, n\_202, n\_203, n\_204, n\_205, n\_206, n\_207, n\_208;

wire n\_209, n\_210, n\_211, n\_212, n\_213, n\_214, n\_215, n\_216;

wire n\_217, n\_218, n\_219, n\_220, n\_221, n\_222, n\_223, n\_224;

wire n\_225, n\_226, n\_227, n\_228, n\_229, n\_230, n\_231, n\_232;

wire n\_233, n\_234, n\_235, n\_236, n\_237, n\_238, n\_239, n\_240;

wire n\_241, n\_242, n\_243, n\_244, n\_245, n\_246, n\_247, n\_248;

wire n\_249, n\_250, n\_251, n\_252, n\_253, n\_254, n\_255, n\_256;

wire n\_257, n\_258, n\_259, n\_260, n\_261, n\_262, n\_263, n\_264;

wire n\_265, n\_266, n\_267, n\_268, n\_269, n\_270, n\_271, n\_272;

wire n\_273, n\_274, n\_275, n\_276, n\_277, n\_278, n\_279, n\_280;

wire n\_281, n\_282, n\_283, n\_284, n\_285, n\_286, n\_287, n\_288;

wire n\_289, n\_290, n\_291, n\_292, n\_293, n\_294, n\_295, n\_296;

wire n\_297, n\_298, n\_299, n\_300, n\_301, n\_302, n\_303, n\_304;

wire n\_305, n\_306, n\_307, n\_308, n\_309, n\_310, n\_311, n\_312;

wire n\_313, n\_314, n\_315, n\_316, n\_317, n\_318, n\_319, n\_320;

wire n\_321, n\_322, n\_323, n\_324, n\_325, n\_326, n\_327, n\_328;

wire n\_329, n\_330, n\_331, n\_332, n\_333, n\_334, n\_335, n\_336;

wire n\_337, n\_338, n\_339, n\_340, n\_341, n\_342, n\_343, n\_344;

wire n\_345, n\_346, n\_347, n\_348, n\_349, n\_350, n\_351, n\_352;

wire n\_353, n\_354, n\_355, n\_356, n\_357, n\_358, n\_359, n\_360;

wire n\_361, n\_362, n\_363, n\_364, n\_365, n\_366, n\_367, n\_368;

wire n\_369, n\_370, n\_371, n\_372, n\_373, n\_374, n\_375, n\_376;

wire n\_377, n\_378, n\_379, n\_380, n\_381, n\_382, n\_383, n\_384;

wire n\_385, n\_386, n\_387, n\_388, n\_389, n\_390, n\_391, n\_392;

wire n\_393, n\_394, n\_395, n\_396, n\_397, n\_398, n\_399, n\_400;

wire n\_401, n\_402, n\_403, n\_404, n\_405, n\_406, n\_407, n\_408;

wire n\_409, n\_410, n\_411, n\_412, n\_413, n\_414, n\_415, n\_416;

wire n\_417, n\_418, n\_419, n\_420, n\_421, n\_422, n\_423, n\_424;

wire n\_425, n\_426, n\_427, n\_428, n\_430;

DFFSNQ\_X1 \savings\_local\_reg[0] (.SN (1'b1), .CLK (clk), .D (n\_430),

.Q (savings\_local[0]));

NOR2\_X1 g12433(.A1 (n\_428), .A2 (rst), .ZN (n\_430));

DFFSNQ\_X1 \chequing\_local\_reg[0] (.SN (1'b1), .CLK (clk), .D (n\_423),

.Q (chequing\_local[0]));

DFFSNQ\_X1 \savings\_local\_reg[3] (.SN (1'b1), .CLK (clk), .D (n\_427),

.Q (savings\_local[3]));

DFFSNQ\_X1 \savings\_local\_reg[5] (.SN (1'b1), .CLK (clk), .D (n\_426),

.Q (savings\_local[5]));

DFFSNQ\_X1 \savings\_local\_reg[6] (.SN (1'b1), .CLK (clk), .D (n\_424),

.Q (savings\_local[6]));

DFFSNQ\_X1 \savings\_local\_reg[7] (.SN (1'b1), .CLK (clk), .D (n\_422),

.Q (savings\_local[7]));

DFFSNQ\_X1 \savings\_local\_reg[8] (.SN (1'b1), .CLK (clk), .D (n\_421),

.Q (savings\_local[8]));

DFFSNQ\_X1 \savings\_local\_reg[9] (.SN (1'b1), .CLK (clk), .D (n\_420),

.Q (savings\_local[9]));

AOI22\_X1 g12461(.A1 (n\_401), .A2 (n\_163), .B1 (n\_402), .B2

(savings\_local[0]), .ZN (n\_428));

DFFSNQ\_X1 \chequing\_local\_reg[10] (.SN (1'b1), .CLK (clk), .D

(n\_411), .Q (chequing\_local[10]));

DFFSNQ\_X1 \chequing\_local\_reg[5] (.SN (1'b1), .CLK (clk), .D (n\_418),

.Q (chequing\_local[5]));

DFFSNQ\_X1 \chequing\_local\_reg[6] (.SN (1'b1), .CLK (clk), .D (n\_417),

.Q (chequing\_local[6]));

DFFSNQ\_X1 \chequing\_local\_reg[7] (.SN (1'b1), .CLK (clk), .D (n\_416),

.Q (chequing\_local[7]));

DFFSNQ\_X1 \chequing\_local\_reg[8] (.SN (1'b1), .CLK (clk), .D (n\_415),

.Q (chequing\_local[8]));

DFFSNQ\_X1 \chequing\_local\_reg[9] (.SN (1'b1), .CLK (clk), .D (n\_414),

.Q (chequing\_local[9]));

DFFSNQ\_X1 \chequing\_local\_reg[12] (.SN (1'b1), .CLK (clk), .D

(n\_412), .Q (chequing\_local[12]));

DFFSNQ\_X1 \chequing\_local\_reg[11] (.SN (1'b1), .CLK (clk), .D

(n\_413), .Q (chequing\_local[11]));

DFFSNQ\_X1 \chequing\_local\_reg[1] (.SN (1'b1), .CLK (clk), .D (n\_410),

.Q (chequing\_local[1]));

DFFSNQ\_X1 \chequing\_local\_reg[13] (.SN (1'b1), .CLK (clk), .D

(n\_419), .Q (chequing\_local[13]));

DFFSNQ\_X1 \chequing\_local\_reg[2] (.SN (1'b1), .CLK (clk), .D (n\_409),

.Q (chequing\_local[2]));

NAND4\_X1 g12486(.A1 (n\_393), .A2 (n\_347), .A3 (n\_201), .A4 (n\_425),

.ZN (n\_427));

NAND4\_X1 g12487(.A1 (n\_392), .A2 (n\_346), .A3 (n\_234), .A4 (n\_425),

.ZN (n\_426));

NAND4\_X1 g12488(.A1 (n\_390), .A2 (n\_344), .A3 (n\_245), .A4 (n\_425),

.ZN (n\_424));

NAND2\_X1 g12460(.A1 (n\_394), .A2 (n\_404), .ZN (n\_423));

NAND4\_X1 g12489(.A1 (n\_389), .A2 (n\_343), .A3 (n\_255), .A4 (n\_425),

.ZN (n\_422));

NAND4\_X1 g12490(.A1 (n\_388), .A2 (n\_342), .A3 (n\_268), .A4 (n\_425),

.ZN (n\_421));

NAND4\_X1 g12491(.A1 (n\_387), .A2 (n\_341), .A3 (n\_280), .A4 (n\_425),

.ZN (n\_420));

DFFSNQ\_X1 \chequing\_local\_reg[4] (.SN (1'b1), .CLK (clk), .D (n\_399),

.Q (chequing\_local[4]));

DFFSNQ\_X1 \chequing\_local\_reg[3] (.SN (1'b1), .CLK (clk), .D (n\_400),

.Q (chequing\_local[3]));

DFFSNQ\_X1 \savings\_local\_reg[4] (.SN (1'b1), .CLK (clk), .D (n\_407),

.Q (savings\_local[4]));

DFFSNQ\_X1 \savings\_local\_reg[11] (.SN (1'b1), .CLK (clk), .D (n\_405),

.Q (savings\_local[11]));

DFFSNQ\_X1 \savings\_local\_reg[12] (.SN (1'b1), .CLK (clk), .D (n\_397),

.Q (savings\_local[12]));

DFFSNQ\_X1 \savings\_local\_reg[13] (.SN (1'b1), .CLK (clk), .D (n\_398),

.Q (savings\_local[13]));

DFFSNQ\_X1 \savings\_local\_reg[1] (.SN (1'b1), .CLK (clk), .D (n\_396),

.Q (savings\_local[1]));

DFFSNQ\_X1 \savings\_local\_reg[2] (.SN (1'b1), .CLK (clk), .D (n\_395),

.Q (savings\_local[2]));

DFFSNQ\_X1 \savings\_local\_reg[10] (.SN (1'b1), .CLK (clk), .D (n\_408),

.Q (savings\_local[10]));

INV\_X1 g12465(.I (n\_403), .ZN (n\_419));

NAND2\_X1 g12469(.A1 (n\_385), .A2 (n\_371), .ZN (n\_418));

NAND2\_X1 g12470(.A1 (n\_382), .A2 (n\_368), .ZN (n\_417));

NAND2\_X1 g12471(.A1 (n\_381), .A2 (n\_369), .ZN (n\_416));

NAND2\_X1 g12472(.A1 (n\_380), .A2 (n\_367), .ZN (n\_415));

NAND2\_X1 g12473(.A1 (n\_379), .A2 (n\_366), .ZN (n\_414));

NAND2\_X1 g12474(.A1 (n\_378), .A2 (n\_365), .ZN (n\_413));

NAND2\_X1 g12475(.A1 (n\_377), .A2 (n\_364), .ZN (n\_412));

NAND2\_X1 g12476(.A1 (n\_386), .A2 (n\_361), .ZN (n\_411));

NAND2\_X1 g12477(.A1 (n\_376), .A2 (n\_363), .ZN (n\_410));

NAND2\_X1 g12478(.A1 (n\_375), .A2 (n\_362), .ZN (n\_409));

OAI21\_X1 g12484(.A1 (n\_44), .A2 (n\_406), .B (n\_349), .ZN (n\_408));

OAI21\_X1 g12483(.A1 (n\_406), .A2 (n\_204), .B (n\_350), .ZN (n\_407));

OAI21\_X1 g12485(.A1 (n\_41), .A2 (n\_406), .B (n\_348), .ZN (n\_405));

AOI21\_X1 g12492(.A1 (n\_340), .A2 (n\_156), .B (rst), .ZN (n\_404));

AOI21\_X1 g12466(.A1 (chequing\_local[13]), .A2 (n\_370), .B (n\_356),

.ZN (n\_403));

NAND2\_X1 g12511(.A1 (n\_401), .A2 (amount[0]), .ZN (n\_402));

NAND2\_X1 g12467(.A1 (n\_360), .A2 (n\_374), .ZN (n\_400));

NAND2\_X1 g12468(.A1 (n\_359), .A2 (n\_372), .ZN (n\_399));

OAI21\_X1 g12479(.A1 (n\_98), .A2 (n\_406), .B (n\_357), .ZN (n\_398));

OAI21\_X1 g12480(.A1 (n\_313), .A2 (n\_406), .B (n\_355), .ZN (n\_397));

OAI21\_X1 g12481(.A1 (n\_406), .A2 (n\_105), .B (n\_352), .ZN (n\_396));

OAI21\_X1 g12482(.A1 (n\_406), .A2 (n\_32), .B (n\_351), .ZN (n\_395));

OAI21\_X1 g12464(.A1 (n\_373), .A2 (n\_67), .B (chequing\_local[0]), .ZN

(n\_394));

NAND2\_X1 g12505(.A1 (n\_391), .A2 (savings\_local[3]), .ZN (n\_393));

NAND2\_X1 g12506(.A1 (n\_391), .A2 (savings\_local[5]), .ZN (n\_392));

NAND2\_X1 g12507(.A1 (n\_391), .A2 (savings\_local[6]), .ZN (n\_390));

NAND2\_X1 g12508(.A1 (n\_391), .A2 (savings\_local[7]), .ZN (n\_389));

NAND2\_X1 g12509(.A1 (n\_391), .A2 (savings\_local[8]), .ZN (n\_388));

NAND2\_X1 g12510(.A1 (n\_391), .A2 (savings\_local[9]), .ZN (n\_387));

AOI22\_X1 g12524(.A1 (n\_384), .A2 (n\_288), .B1 (n\_290), .B2 (n\_383),

.ZN (n\_386));

DFFSNQ\_X1 open\_atm\_dispense\_reg(.SN (1'b1), .CLK (clk), .D (n\_338),

.Q (open\_atm\_dispense));

AOI22\_X1 g12525(.A1 (n\_384), .A2 (n\_225), .B1 (n\_227), .B2 (n\_383),

.ZN (n\_385));

DFFSNQ\_X1 \state\_reg[0] (.SN (1'b1), .CLK (clk), .D (n\_339), .Q

(state[0]));

AOI22\_X1 g12526(.A1 (n\_384), .A2 (n\_236), .B1 (n\_242), .B2 (n\_383),

.ZN (n\_382));

AOI22\_X1 g12527(.A1 (n\_384), .A2 (n\_254), .B1 (n\_250), .B2 (n\_383),

.ZN (n\_381));

AOI22\_X1 g12528(.A1 (n\_384), .A2 (n\_263), .B1 (n\_265), .B2 (n\_383),

.ZN (n\_380));

AOI22\_X1 g12529(.A1 (n\_384), .A2 (n\_273), .B1 (n\_275), .B2 (n\_383),

.ZN (n\_379));

AOI22\_X1 g12530(.A1 (n\_384), .A2 (n\_296), .B1 (n\_298), .B2 (n\_383),

.ZN (n\_378));

AOI22\_X1 g12531(.A1 (n\_384), .A2 (n\_306), .B1 (n\_308), .B2 (n\_383),

.ZN (n\_377));

AOI22\_X1 g12532(.A1 (n\_384), .A2 (n\_158), .B1 (n\_383), .B2 (n\_159),

.ZN (n\_376));

AOI22\_X1 g12533(.A1 (n\_384), .A2 (n\_176), .B1 (n\_383), .B2 (n\_169),

.ZN (n\_375));

NAND2\_X1 g12493(.A1 (n\_373), .A2 (chequing\_local[3]), .ZN (n\_374));

NAND2\_X1 g12494(.A1 (n\_373), .A2 (chequing\_local[4]), .ZN (n\_372));

NAND2\_X1 g12495(.A1 (n\_370), .A2 (chequing\_local[5]), .ZN (n\_371));

NAND2\_X1 g12496(.A1 (n\_370), .A2 (chequing\_local[7]), .ZN (n\_369));

NAND2\_X1 g12497(.A1 (n\_370), .A2 (chequing\_local[6]), .ZN (n\_368));

NAND2\_X1 g12498(.A1 (n\_370), .A2 (chequing\_local[8]), .ZN (n\_367));

NAND2\_X1 g12499(.A1 (n\_370), .A2 (chequing\_local[9]), .ZN (n\_366));

NAND2\_X1 g12500(.A1 (chequing\_local[11]), .A2 (n\_370), .ZN (n\_365));

NAND2\_X1 g12501(.A1 (chequing\_local[12]), .A2 (n\_370), .ZN (n\_364));

NAND2\_X1 g12502(.A1 (n\_370), .A2 (chequing\_local[1]), .ZN (n\_363));

NAND2\_X1 g12503(.A1 (n\_370), .A2 (chequing\_local[2]), .ZN (n\_362));

NAND2\_X1 g12504(.A1 (chequing\_local[10]), .A2 (n\_370), .ZN (n\_361));

AOI21\_X1 g12514(.A1 (n\_358), .A2 (n\_197), .B (n\_207), .ZN (n\_360));

AOI21\_X1 g12515(.A1 (n\_358), .A2 (n\_213), .B (n\_228), .ZN (n\_359));

AOI22\_X1 g12516(.A1 (n\_354), .A2 (n\_318), .B1 (n\_323), .B2 (n\_353),

.ZN (n\_357));

OAI22\_X1 g12517(.A1 (n\_334), .A2 (n\_320), .B1 (n\_321), .B2 (n\_182),

.ZN (n\_356));

AOI22\_X1 g12518(.A1 (n\_354), .A2 (n\_311), .B1 (n\_312), .B2 (n\_353),

.ZN (n\_355));

AOI22\_X1 g12519(.A1 (n\_354), .A2 (n\_164), .B1 (n\_162), .B2 (n\_353),

.ZN (n\_352));

AOI22\_X1 g12520(.A1 (n\_354), .A2 (n\_174), .B1 (n\_172), .B2 (n\_353),

.ZN (n\_351));

AOI22\_X1 g12521(.A1 (n\_354), .A2 (n\_211), .B1 (n\_215), .B2 (n\_353),

.ZN (n\_350));

AOI22\_X1 g12522(.A1 (n\_354), .A2 (n\_283), .B1 (n\_285), .B2 (n\_353),

.ZN (n\_349));

AOI22\_X1 g12523(.A1 (n\_354), .A2 (n\_300), .B1 (n\_293), .B2 (n\_353),

.ZN (n\_348));

INV\_X1 g12534(.I (n\_391), .ZN (n\_401));

NAND2\_X1 g12536(.A1 (n\_345), .A2 (n\_194), .ZN (n\_347));

NAND2\_X1 g12537(.A1 (n\_345), .A2 (n\_220), .ZN (n\_346));

NAND2\_X1 g12538(.A1 (n\_345), .A2 (n\_238), .ZN (n\_344));

NAND2\_X1 g12539(.A1 (n\_345), .A2 (n\_252), .ZN (n\_343));

NAND2\_X1 g12540(.A1 (n\_345), .A2 (n\_260), .ZN (n\_342));

NAND2\_X1 g12541(.A1 (n\_345), .A2 (n\_277), .ZN (n\_341));

INV\_X1 g12543(.I (n\_373), .ZN (n\_340));

NAND2\_X1 g12512(.A1 (n\_337), .A2 (n\_187), .ZN (n\_339));

NAND2\_X1 g12513(.A1 (n\_337), .A2 (n\_181), .ZN (n\_338));

NOR2\_X1 g12535(.A1 (n\_345), .A2 (n\_279), .ZN (n\_391));

OAI22\_X1 g12544(.A1 (state[0]), .A2 (n\_336), .B1 (n\_332), .B2

(n\_335), .ZN (n\_373));

AOI22\_X1 g12545(.A1 (n\_331), .A2 (n\_333), .B1 (n\_186), .B2 (n\_166),

.ZN (n\_406));

OAI22\_X1 g12546(.A1 (n\_336), .A2 (n\_330), .B1 (n\_216), .B2 (n\_335),

.ZN (n\_370));

INV\_X1 g12548(.I (n\_334), .ZN (n\_384));

NAND4\_X1 g12542(.A1 (n\_143), .A2 (n\_328), .A3 (n\_326), .A4 (n\_333),

.ZN (n\_337));

AND2\_X1 g12547(.A1 (n\_332), .A2 (n\_336), .Z (n\_358));

NAND2\_X1 g12549(.A1 (n\_336), .A2 (n\_333), .ZN (n\_334));

NOR2\_X1 g12550(.A1 (state[0]), .A2 (n\_331), .ZN (n\_345));

NOR2\_X1 g12551(.A1 (n\_331), .A2 (n\_330), .ZN (n\_354));

NOR3\_X1 g12554(.A1 (n\_329), .A2 (n\_325), .A3 (account\_selection), .ZN

(n\_336));

OR3\_X2 g12555(.A1 (n\_329), .A2 (n\_327), .A3 (n\_324), .Z (n\_331));

NAND2\_X1 g12552(.A1 (n\_327), .A2 (account\_selection), .ZN (n\_328));

NAND2\_X1 g12553(.A1 (n\_325), .A2 (n\_324), .ZN (n\_326));

XOR2\_X1 g12558(.A1 (n\_315), .A2 (n\_316), .Z (n\_323));

OAI22\_X1 g12556(.A1 (n\_319), .A2 (n\_111), .B1 (chequing\_local[13]),

.B2 (n\_322), .ZN (n\_325));

OAI22\_X1 g12557(.A1 (n\_317), .A2 (n\_73), .B1 (savings\_local[13]), .B2

(n\_322), .ZN (n\_327));

XNOR2\_X1 g12559(.A1 (n\_314), .A2 (n\_144), .ZN (n\_321));

NAND2\_X1 g12560(.A1 (n\_319), .A2 (n\_145), .ZN (n\_320));

AND2\_X1 g12561(.A1 (n\_317), .A2 (n\_316), .Z (n\_318));

OAI21\_X1 g12563(.A1 (n\_303), .A2 (n\_125), .B (n\_47), .ZN (n\_315));

AOI22\_X1 g12562(.A1 (n\_307), .A2 (n\_21), .B1 (chequing\_local[12]),

.B2 (amount[12]), .ZN (n\_314));

OAI21\_X1 g12564(.A1 (n\_305), .A2 (n\_80), .B (n\_135), .ZN (n\_319));

OAI22\_X1 g12565(.A1 (n\_310), .A2 (n\_36), .B1 (n\_313), .B2

(amount[12]), .ZN (n\_317));

XOR2\_X1 g12566(.A1 (n\_302), .A2 (n\_309), .Z (n\_312));

XOR2\_X1 g12567(.A1 (n\_310), .A2 (n\_309), .Z (n\_311));

XOR2\_X1 g12568(.A1 (n\_307), .A2 (n\_304), .Z (n\_308));

XOR2\_X1 g12569(.A1 (n\_305), .A2 (n\_304), .Z (n\_306));

INV\_X1 g12570(.I (n\_302), .ZN (n\_303));

OAI21\_X1 g12571(.A1 (n\_292), .A2 (n\_51), .B (n\_126), .ZN (n\_302));

OAI21\_X1 g12572(.A1 (n\_297), .A2 (n\_57), .B (n\_122), .ZN (n\_307));

AOI22\_X1 g12573(.A1 (n\_295), .A2 (n\_27), .B1 (chequing\_local[11]),

.B2 (n\_301), .ZN (n\_305));

AOI22\_X1 g12574(.A1 (n\_299), .A2 (n\_42), .B1 (savings\_local[11]), .B2

(n\_301), .ZN (n\_310));

XOR2\_X1 g12575(.A1 (n\_299), .A2 (n\_291), .Z (n\_300));

XOR2\_X1 g12576(.A1 (n\_297), .A2 (n\_294), .Z (n\_298));

XOR2\_X1 g12577(.A1 (n\_295), .A2 (n\_294), .Z (n\_296));

XOR2\_X1 g12578(.A1 (n\_292), .A2 (n\_291), .Z (n\_293));

AOI22\_X1 g12579(.A1 (n\_289), .A2 (n\_19), .B1 (chequing\_local[10]),

.B2 (amount[10]), .ZN (n\_297));

AOI22\_X1 g12580(.A1 (n\_284), .A2 (n\_45), .B1 (savings\_local[10]), .B2

(amount[10]), .ZN (n\_292));

OAI21\_X1 g12581(.A1 (n\_287), .A2 (n\_109), .B (n\_137), .ZN (n\_295));

OAI21\_X1 g12582(.A1 (n\_282), .A2 (n\_90), .B (n\_134), .ZN (n\_299));

XOR2\_X1 g12583(.A1 (n\_289), .A2 (n\_286), .Z (n\_290));

XOR2\_X1 g12584(.A1 (n\_287), .A2 (n\_286), .Z (n\_288));

XOR2\_X1 g12585(.A1 (n\_284), .A2 (n\_281), .Z (n\_285));

XOR2\_X1 g12586(.A1 (n\_282), .A2 (n\_281), .Z (n\_283));

NAND2\_X1 g12587(.A1 (n\_270), .A2 (n\_279), .ZN (n\_280));

OAI21\_X1 g12588(.A1 (n\_274), .A2 (n\_76), .B (n\_123), .ZN (n\_289));

OAI21\_X1 g12589(.A1 (n\_267), .A2 (n\_121), .B (n\_55), .ZN (n\_284));

AOI22\_X1 g12590(.A1 (n\_272), .A2 (n\_25), .B1 (chequing\_local[9]), .B2

(n\_278), .ZN (n\_287));

AOI22\_X1 g12591(.A1 (n\_276), .A2 (n\_35), .B1 (savings\_local[9]), .B2

(n\_278), .ZN (n\_282));

XNOR2\_X1 g12593(.A1 (n\_276), .A2 (n\_269), .ZN (n\_277));

XOR2\_X1 g12594(.A1 (n\_274), .A2 (n\_271), .Z (n\_275));

XOR2\_X1 g12595(.A1 (n\_272), .A2 (n\_271), .Z (n\_273));

XOR2\_X1 g12592(.A1 (n\_266), .A2 (n\_269), .Z (n\_270));

NAND2\_X1 g12596(.A1 (n\_258), .A2 (n\_279), .ZN (n\_268));

INV\_X1 g12597(.I (n\_266), .ZN (n\_267));

OAI21\_X1 g12599(.A1 (n\_262), .A2 (n\_99), .B (n\_141), .ZN (n\_272));

AOI22\_X1 g12600(.A1 (n\_264), .A2 (n\_17), .B1 (chequing\_local[8]), .B2

(amount[8]), .ZN (n\_274));

OAI22\_X1 g12601(.A1 (n\_259), .A2 (n\_37), .B1 (n\_11), .B2 (amount[8]),

.ZN (n\_276));

XOR2\_X1 g12603(.A1 (n\_264), .A2 (n\_261), .Z (n\_265));

XOR2\_X1 g12604(.A1 (n\_262), .A2 (n\_261), .Z (n\_263));

XNOR2\_X1 g12605(.A1 (n\_259), .A2 (n\_256), .ZN (n\_260));

OAI21\_X1 g12598(.A1 (n\_257), .A2 (n\_63), .B (n\_120), .ZN (n\_266));

XOR2\_X1 g12602(.A1 (n\_257), .A2 (n\_256), .Z (n\_258));

NAND2\_X1 g12606(.A1 (n\_248), .A2 (n\_279), .ZN (n\_255));

NAND2\_X1 g12607(.A1 (n\_244), .A2 (n\_24), .ZN (n\_264));

AOI21\_X1 g12608(.A1 (n\_253), .A2 (n\_112), .B (n\_89), .ZN (n\_262));

AOI22\_X1 g12610(.A1 (n\_251), .A2 (n\_29), .B1 (savings\_local[7]), .B2

(n\_68), .ZN (n\_259));

XNOR2\_X1 g12613(.A1 (n\_253), .A2 (n\_249), .ZN (n\_254));

XNOR2\_X1 g12614(.A1 (n\_251), .A2 (n\_246), .ZN (n\_252));

AOI21\_X1 g12609(.A1 (n\_247), .A2 (n\_50), .B (n\_118), .ZN (n\_257));

XOR2\_X1 g12611(.A1 (n\_243), .A2 (n\_249), .Z (n\_250));

XOR2\_X1 g12612(.A1 (n\_247), .A2 (n\_246), .Z (n\_248));

NAND2\_X1 g12616(.A1 (n\_240), .A2 (n\_279), .ZN (n\_245));

OAI21\_X1 g12615(.A1 (chequing\_local[7]), .A2 (amount[7]), .B (n\_243),

.ZN (n\_244));

OAI21\_X1 g12619(.A1 (n\_10), .A2 (amount[6]), .B (n\_233), .ZN (n\_253));

OAI21\_X1 g12620(.A1 (n\_12), .A2 (amount[6]), .B (n\_231), .ZN (n\_251));

OAI21\_X1 g12618(.A1 (n\_239), .A2 (n\_74), .B (n\_114), .ZN (n\_247));

OAI21\_X1 g12617(.A1 (n\_241), .A2 (n\_78), .B (n\_116), .ZN (n\_243));

XOR2\_X1 g12621(.A1 (n\_241), .A2 (n\_235), .Z (n\_242));

XOR2\_X1 g12622(.A1 (n\_239), .A2 (n\_237), .Z (n\_240));

XOR2\_X1 g12623(.A1 (n\_229), .A2 (n\_237), .Z (n\_238));

XOR2\_X1 g12624(.A1 (n\_232), .A2 (n\_235), .Z (n\_236));

NAND2\_X1 g12625(.A1 (n\_222), .A2 (n\_279), .ZN (n\_234));

OAI21\_X1 g12626(.A1 (chequing\_local[6]), .A2 (n\_230), .B (n\_232), .ZN

(n\_233));

OAI21\_X1 g12627(.A1 (savings\_local[6]), .A2 (n\_230), .B (n\_229), .ZN

(n\_231));

DFFSNQ\_X1 \state\_reg[1] (.SN (1'b1), .CLK (clk), .D (n\_217), .Q

(state[1]));

AOI22\_X1 g12628(.A1 (n\_226), .A2 (n\_18), .B1 (chequing\_local[5]), .B2

(amount[5]), .ZN (n\_241));

AOI22\_X1 g12629(.A1 (n\_221), .A2 (n\_15), .B1 (savings\_local[5]), .B2

(amount[5]), .ZN (n\_239));

OAI21\_X1 g12630(.A1 (n\_224), .A2 (n\_84), .B (n\_142), .ZN (n\_232));

OAI21\_X1 g12631(.A1 (n\_219), .A2 (n\_86), .B (n\_133), .ZN (n\_229));

OAI21\_X1 g12632(.A1 (n\_214), .A2 (n\_206), .B (n\_425), .ZN (n\_228));

XOR2\_X1 g12633(.A1 (n\_226), .A2 (n\_223), .Z (n\_227));

XOR2\_X1 g12634(.A1 (n\_224), .A2 (n\_223), .Z (n\_225));

XOR2\_X1 g12635(.A1 (n\_221), .A2 (n\_218), .Z (n\_222));

XOR2\_X1 g12636(.A1 (n\_219), .A2 (n\_218), .Z (n\_220));

OAI22\_X1 g12643(.A1 (n\_200), .A2 (n\_216), .B1 (n\_148), .B2 (n\_330),

.ZN (n\_217));

XOR2\_X1 g12644(.A1 (n\_205), .A2 (n\_210), .Z (n\_215));

XOR2\_X1 g12645(.A1 (n\_209), .A2 (n\_212), .Z (n\_214));

XNOR2\_X1 g12646(.A1 (n\_203), .A2 (n\_212), .ZN (n\_213));

XOR2\_X1 g12647(.A1 (n\_208), .A2 (n\_210), .Z (n\_211));

OAI21\_X1 g12638(.A1 (n\_209), .A2 (n\_119), .B (n\_70), .ZN (n\_226));

AOI21\_X1 g12639(.A1 (n\_208), .A2 (n\_107), .B (n\_138), .ZN (n\_219));

OAI21\_X1 g12640(.A1 (n\_199), .A2 (n\_206), .B (n\_425), .ZN (n\_207));

OAI22\_X1 g12641(.A1 (n\_205), .A2 (n\_20), .B1 (n\_204), .B2 (n\_202),

.ZN (n\_221));

AOI22\_X1 g12642(.A1 (n\_203), .A2 (n\_34), .B1 (chequing\_local[4]), .B2

(n\_202), .ZN (n\_224));

NAND2\_X1 g12648(.A1 (n\_192), .A2 (n\_279), .ZN (n\_201));

DFFSNQ\_X1 \state\_reg[2] (.SN (1'b1), .CLK (clk), .D (n\_189), .Q

(state[2]));

AOI21\_X1 g12650(.A1 (n\_188), .A2 (n\_185), .B (n\_154), .ZN (n\_200));

AOI22\_X1 g12651(.A1 (n\_191), .A2 (n\_22), .B1 (savings\_local[3]), .B2

(amount[3]), .ZN (n\_205));

OAI21\_X1 g12652(.A1 (n\_193), .A2 (n\_94), .B (n\_139), .ZN (n\_208));

OAI21\_X1 g12653(.A1 (n\_196), .A2 (n\_82), .B (n\_136), .ZN (n\_203));

AOI22\_X1 g12654(.A1 (n\_198), .A2 (n\_23), .B1 (chequing\_local[3]), .B2

(amount[3]), .ZN (n\_209));

XNOR2\_X1 g12655(.A1 (n\_198), .A2 (n\_195), .ZN (n\_199));

XOR2\_X1 g12656(.A1 (n\_196), .A2 (n\_195), .Z (n\_197));

XOR2\_X1 g12657(.A1 (n\_193), .A2 (n\_190), .Z (n\_194));

XOR2\_X1 g12658(.A1 (n\_191), .A2 (n\_190), .Z (n\_192));

OAI22\_X1 g12660(.A1 (n\_165), .A2 (rst), .B1 (n\_188), .B2 (n\_216), .ZN

(n\_189));

DFFSNQ\_X1 open\_atm\_receive\_reg(.SN (1'b1), .CLK (clk), .D (n\_184), .Q

(open\_atm\_receive));

DFFSNQ\_X1 \state\_reg[3] (.SN (1'b1), .CLK (clk), .D (n\_183), .Q

(state[3]));

AOI22\_X1 g12661(.A1 (n\_177), .A2 (n\_160), .B1 (n\_103), .B2 (n\_186),

.ZN (n\_187));

OAI21\_X1 g12665(.A1 (n\_149), .A2 (n\_147), .B (n\_150), .ZN (n\_185));

INV\_X1 g12669(.I (n\_179), .ZN (n\_184));

OAI21\_X1 g12675(.A1 (n\_113), .A2 (n\_216), .B (n\_155), .ZN (n\_183));

INV\_X1 g12680(.I (n\_182), .ZN (n\_383));

OAI21\_X1 g12663(.A1 (n\_178), .A2 (n\_16), .B (open\_atm\_dispense), .ZN

(n\_181));

OAI21\_X1 g12664(.A1 (n\_170), .A2 (n\_61), .B (n\_124), .ZN (n\_191));

OAI21\_X1 g12666(.A1 (n\_167), .A2 (n\_53), .B (n\_115), .ZN (n\_198));

AOI22\_X1 g12667(.A1 (n\_173), .A2 (n\_33), .B1 (savings\_local[2]), .B2

(n\_180), .ZN (n\_193));

AOI22\_X1 g12668(.A1 (n\_175), .A2 (n\_30), .B1 (chequing\_local[2]), .B2

(n\_180), .ZN (n\_196));

AOI22\_X1 g12670(.A1 (open\_atm\_receive), .A2 (n\_178), .B1 (n\_146), .B2

(n\_177), .ZN (n\_179));

XOR2\_X1 g12671(.A1 (n\_168), .A2 (n\_175), .Z (n\_176));

XOR2\_X1 g12672(.A1 (n\_171), .A2 (n\_173), .Z (n\_174));

XOR2\_X1 g12673(.A1 (n\_171), .A2 (n\_170), .Z (n\_172));

XOR2\_X1 g12674(.A1 (n\_168), .A2 (n\_167), .Z (n\_169));

NOR2\_X1 g12676(.A1 (n\_332), .A2 (n\_166), .ZN (n\_279));

NOR2\_X1 g12677(.A1 (n\_216), .A2 (n\_166), .ZN (n\_353));

NAND2\_X1 g12678(.A1 (state[0]), .A2 (n\_335), .ZN (n\_206));

AOI21\_X1 g12679(.A1 (n\_153), .A2 (n\_7), .B (n\_152), .ZN (n\_165));

NAND2\_X1 g12681(.A1 (n\_186), .A2 (n\_335), .ZN (n\_182));

XOR2\_X1 g12683(.A1 (n\_161), .A2 (n\_163), .Z (n\_164));

XNOR2\_X1 g12684(.A1 (n\_161), .A2 (n\_104), .ZN (n\_162));

NAND3\_X1 g12682(.A1 (n\_151), .A2 (n\_101), .A3 (n\_128), .ZN (n\_160));

XOR2\_X1 g12685(.A1 (n\_157), .A2 (n\_129), .Z (n\_159));

XNOR2\_X1 g12686(.A1 (n\_157), .A2 (n\_156), .ZN (n\_158));

AOI21\_X1 g12694(.A1 (n\_154), .A2 (n\_333), .B (n\_132), .ZN (n\_155));

NAND2\_X1 g12687(.A1 (n\_153), .A2 (account\_selection), .ZN (n\_166));

AND2\_X1 g12688(.A1 (n\_153), .A2 (n\_324), .Z (n\_335));

OAI22\_X1 g12692(.A1 (n\_151), .A2 (n\_43), .B1 (n\_150), .B2 (n\_102),

.ZN (n\_152));

NAND4\_X1 g12695(.A1 (n\_97), .A2 (n\_14), .A3 (pin[7]), .A4 (pin[6]),

.ZN (n\_149));

AOI21\_X1 g12698(.A1 (n\_151), .A2 (state[3]), .B (n\_127), .ZN (n\_148));

INV\_X1 g12689(.I (n\_130), .ZN (n\_167));

OAI21\_X1 g12691(.A1 (n\_163), .A2 (n\_92), .B (n\_140), .ZN (n\_173));

NAND3\_X1 g12693(.A1 (n\_96), .A2 (n\_4), .A3 (pin[1]), .ZN (n\_147));

OAI21\_X1 g12696(.A1 (n\_146), .A2 (rst), .B (n\_216), .ZN (n\_178));

AOI21\_X1 g12699(.A1 (savings\_local[1]), .A2 (amount[1]), .B (n\_106),

.ZN (n\_170));

OAI22\_X1 g12700(.A1 (n\_156), .A2 (n\_38), .B1 (n\_8), .B2 (amount[1]),

.ZN (n\_175));

INV\_X1 g12701(.I (n\_144), .ZN (n\_145));

INV\_X1 g12720(.I (n\_329), .ZN (n\_143));

NAND2\_X1 g12722(.A1 (n\_142), .A2 (n\_85), .ZN (n\_223));

NAND2\_X1 g12723(.A1 (n\_141), .A2 (n\_100), .ZN (n\_261));

NAND2\_X1 g12724(.A1 (n\_140), .A2 (n\_93), .ZN (n\_161));

NAND2\_X1 g12725(.A1 (n\_139), .A2 (n\_95), .ZN (n\_190));

NOR2\_X1 g12727(.A1 (n\_108), .A2 (n\_138), .ZN (n\_210));

NAND2\_X1 g12728(.A1 (n\_137), .A2 (n\_110), .ZN (n\_286));

NAND2\_X1 g12729(.A1 (n\_136), .A2 (n\_83), .ZN (n\_195));

NAND2\_X1 g12730(.A1 (n\_135), .A2 (n\_81), .ZN (n\_304));

NAND2\_X1 g12731(.A1 (n\_134), .A2 (n\_91), .ZN (n\_281));

NAND2\_X1 g12732(.A1 (n\_133), .A2 (n\_87), .ZN (n\_218));

NOR3\_X1 g12735(.A1 (n\_150), .A2 (n\_66), .A3 (rst), .ZN (n\_132));

AND3\_X1 g12697(.A1 (n\_332), .A2 (n\_150), .A3 (n\_188), .Z (ready));

OAI21\_X1 g12690(.A1 (n\_59), .A2 (n\_129), .B (n\_117), .ZN (n\_130));

NAND2\_X1 g12703(.A1 (n\_127), .A2 (deposit\_withdrawal\_selection), .ZN

(n\_128));

NAND2\_X1 g12704(.A1 (n\_52), .A2 (n\_126), .ZN (n\_291));

NOR2\_X1 g12705(.A1 (n\_48), .A2 (n\_125), .ZN (n\_309));

NAND2\_X1 g12706(.A1 (n\_62), .A2 (n\_124), .ZN (n\_171));

NAND2\_X1 g12707(.A1 (n\_77), .A2 (n\_123), .ZN (n\_271));

NAND2\_X1 g12708(.A1 (n\_58), .A2 (n\_122), .ZN (n\_294));

NOR2\_X1 g12709(.A1 (n\_56), .A2 (n\_121), .ZN (n\_269));

NAND2\_X1 g12710(.A1 (n\_64), .A2 (n\_120), .ZN (n\_256));

NOR2\_X1 g12711(.A1 (n\_71), .A2 (n\_119), .ZN (n\_212));

NOR2\_X1 g12712(.A1 (n\_118), .A2 (n\_49), .ZN (n\_246));

NAND2\_X1 g12713(.A1 (n\_60), .A2 (n\_117), .ZN (n\_157));

NAND2\_X1 g12714(.A1 (n\_79), .A2 (n\_116), .ZN (n\_235));

NAND2\_X1 g12715(.A1 (n\_54), .A2 (n\_115), .ZN (n\_168));

NAND2\_X1 g12716(.A1 (n\_75), .A2 (n\_114), .ZN (n\_237));

AND2\_X1 g12717(.A1 (n\_127), .A2 (n\_150), .Z (n\_153));

NOR2\_X1 g12718(.A1 (n\_146), .A2 (state[3]), .ZN (n\_113));

NOR2\_X1 g12719(.A1 (state[3]), .A2 (n\_330), .ZN (n\_177));

NAND2\_X1 g12721(.A1 (n\_127), .A2 (state[3]), .ZN (n\_329));

NAND2\_X1 g12726(.A1 (n\_88), .A2 (n\_112), .ZN (n\_249));

HA\_X1 g12702(.A (n\_322), .B (chequing\_local[13]), .CO (n\_111), .S

(n\_144));

INV\_X1 g12820(.I (n\_109), .ZN (n\_110));

INV\_X1 g12847(.I (n\_107), .ZN (n\_108));

AOI21\_X1 g12733(.A1 (n\_105), .A2 (n\_46), .B (n\_104), .ZN (n\_106));

OAI21\_X1 g12734(.A1 (n\_150), .A2 (n\_65), .B (n\_102), .ZN (n\_103));

AOI22\_X1 g12736(.A1 (n\_40), .A2 (bank\_card\_insert), .B1 (state[2]),

.B2 (account\_selection), .ZN (n\_101));

INV\_X1 g12816(.I (n\_99), .ZN (n\_100));

AOI22\_X1 g12737(.A1 (n\_98), .A2 (n\_322), .B1 (savings\_local[13]), .B2

(amount[13]), .ZN (n\_316));

NOR4\_X1 g12738(.A1 (n\_0), .A2 (pin[5]), .A3 (pin[3]), .A4 (pin[2]),

.ZN (n\_97));

NOR4\_X1 g12739(.A1 (n\_1), .A2 (pin[11]), .A3 (pin[13]), .A4

(pin[12]), .ZN (n\_96));

INV\_X1 g12840(.I (n\_94), .ZN (n\_95));

INV\_X1 g12802(.I (n\_146), .ZN (n\_151));

INV\_X1 g12811(.I (n\_92), .ZN (n\_93));

INV\_X1 g12813(.I (n\_90), .ZN (n\_91));

INV\_X1 g12818(.I (n\_88), .ZN (n\_89));

INV\_X1 g12824(.I (n\_86), .ZN (n\_87));

INV\_X1 g12833(.I (n\_84), .ZN (n\_85));

INV\_X1 g12843(.I (n\_82), .ZN (n\_83));

INV\_X1 g12850(.I (n\_216), .ZN (n\_186));

INV\_X1 g12804(.I (n\_80), .ZN (n\_81));

INV\_X1 g12799(.I (n\_330), .ZN (n\_333));

NAND2\_X1 g12851(.A1 (state[0]), .A2 (n\_425), .ZN (n\_216));

NOR2\_X1 g12825(.A1 (savings\_local[5]), .A2 (n\_72), .ZN (n\_86));

NOR2\_X1 g12821(.A1 (chequing\_local[10]), .A2 (n\_69), .ZN (n\_109));

INV\_X1 g12781(.I (n\_78), .ZN (n\_79));

INV\_X1 g12794(.I (n\_76), .ZN (n\_77));

INV\_X1 g12761(.I (n\_74), .ZN (n\_75));

NOR2\_X1 g12829(.A1 (n\_98), .A2 (amount[13]), .ZN (n\_73));

NAND2\_X1 g12842(.A1 (chequing\_local[8]), .A2 (n\_39), .ZN (n\_141));

NOR2\_X1 g12834(.A1 (chequing\_local[5]), .A2 (n\_72), .ZN (n\_84));

INV\_X1 g12789(.I (n\_70), .ZN (n\_71));

NAND2\_X1 g12810(.A1 (chequing\_local[10]), .A2 (n\_69), .ZN (n\_137));

NOR2\_X1 g12774(.A1 (n\_28), .A2 (n\_68), .ZN (n\_118));

NOR2\_X1 g12740(.A1 (chequing\_local[0]), .A2 (n\_67), .ZN (n\_156));

NOR2\_X1 g12741(.A1 (n\_65), .A2 (bank\_card\_insert), .ZN (n\_66));

NOR2\_X1 g12742(.A1 (savings\_local[0]), .A2 (n\_67), .ZN (n\_163));

INV\_X1 g12746(.I (n\_63), .ZN (n\_64));

INV\_X1 g12751(.I (n\_61), .ZN (n\_62));

INV\_X1 g12753(.I (n\_59), .ZN (n\_60));

INV\_X1 g12757(.I (n\_57), .ZN (n\_58));

NOR2\_X1 g12844(.A1 (chequing\_local[3]), .A2 (n\_31), .ZN (n\_82));

INV\_X1 g12763(.I (n\_55), .ZN (n\_56));

INV\_X1 g12766(.I (n\_53), .ZN (n\_54));

INV\_X1 g12769(.I (n\_51), .ZN (n\_52));

INV\_X1 g12771(.I (n\_49), .ZN (n\_50));

NAND2\_X1 g12819(.A1 (chequing\_local[7]), .A2 (n\_68), .ZN (n\_88));

INV\_X1 g12779(.I (n\_47), .ZN (n\_48));

NOR2\_X1 g12812(.A1 (savings\_local[1]), .A2 (n\_46), .ZN (n\_92));

NAND2\_X1 g12788(.A1 (n\_44), .A2 (n\_69), .ZN (n\_45));

INV\_X1 g12792(.I (n\_102), .ZN (n\_154));

NAND2\_X1 g12848(.A1 (n\_204), .A2 (amount[4]), .ZN (n\_107));

NOR2\_X1 g12743(.A1 (n\_150), .A2 (bank\_card\_insert), .ZN (n\_43));

NAND2\_X1 g12801(.A1 (n\_41), .A2 (amount[11]), .ZN (n\_42));

NOR2\_X1 g12803(.A1 (n\_65), .A2 (state[1]), .ZN (n\_146));

NOR2\_X1 g12806(.A1 (n\_40), .A2 (state[2]), .ZN (n\_127));

NAND2\_X1 g12809(.A1 (savings\_local[1]), .A2 (n\_46), .ZN (n\_140));

NOR2\_X1 g12814(.A1 (savings\_local[10]), .A2 (n\_69), .ZN (n\_90));

NOR2\_X1 g12815(.A1 (n\_204), .A2 (amount[4]), .ZN (n\_138));

NOR2\_X1 g12817(.A1 (chequing\_local[8]), .A2 (n\_39), .ZN (n\_99));

NAND2\_X1 g12822(.A1 (n\_5), .A2 (amount[7]), .ZN (n\_112));

NOR2\_X1 g12823(.A1 (chequing\_local[1]), .A2 (n\_46), .ZN (n\_38));

NOR2\_X1 g12827(.A1 (savings\_local[8]), .A2 (n\_39), .ZN (n\_37));

NOR2\_X1 g12830(.A1 (savings\_local[12]), .A2 (n\_26), .ZN (n\_36));

NAND2\_X1 g12832(.A1 (n\_2), .A2 (amount[9]), .ZN (n\_35));

NAND2\_X1 g12836(.A1 (n\_3), .A2 (amount[4]), .ZN (n\_34));

NAND2\_X1 g12837(.A1 (n\_32), .A2 (amount[2]), .ZN (n\_33));

NAND2\_X1 g12838(.A1 (chequing\_local[5]), .A2 (n\_72), .ZN (n\_142));

NAND2\_X1 g12839(.A1 (savings\_local[5]), .A2 (n\_72), .ZN (n\_133));

NOR2\_X1 g12841(.A1 (savings\_local[3]), .A2 (n\_31), .ZN (n\_94));

NAND2\_X1 g12846(.A1 (n\_9), .A2 (amount[2]), .ZN (n\_30));

NAND2\_X1 g12835(.A1 (savings\_local[10]), .A2 (n\_69), .ZN (n\_134));

NAND2\_X1 g12808(.A1 (n\_28), .A2 (amount[7]), .ZN (n\_29));

NAND2\_X1 g12845(.A1 (savings\_local[3]), .A2 (n\_31), .ZN (n\_139));

NAND2\_X1 g12807(.A1 (chequing\_local[3]), .A2 (n\_31), .ZN (n\_136));

NAND2\_X1 g12826(.A1 (n\_13), .A2 (amount[11]), .ZN (n\_27));

NAND2\_X1 g12831(.A1 (chequing\_local[12]), .A2 (n\_26), .ZN (n\_135));

NOR2\_X1 g12805(.A1 (chequing\_local[12]), .A2 (n\_26), .ZN (n\_80));

NAND2\_X1 g12800(.A1 (n\_332), .A2 (n\_425), .ZN (n\_330));

NAND2\_X1 g12828(.A1 (n\_6), .A2 (amount[9]), .ZN (n\_25));

NAND2\_X1 g12783(.A1 (chequing\_local[11]), .A2 (amount[11]), .ZN

(n\_122));

NAND2\_X1 g12778(.A1 (chequing\_local[7]), .A2 (amount[7]), .ZN (n\_24));

NOR2\_X1 g12782(.A1 (chequing\_local[6]), .A2 (amount[6]), .ZN (n\_78));

NAND2\_X1 g12797(.A1 (savings\_local[8]), .A2 (amount[8]), .ZN (n\_120));

NAND2\_X1 g12793(.A1 (state[1]), .A2 (state[2]), .ZN (n\_102));

OR2\_X1 g12765(.A1 (chequing\_local[3]), .A2 (amount[3]), .Z (n\_23));

OR2\_X1 g12755(.A1 (savings\_local[3]), .A2 (amount[3]), .Z (n\_22));

NOR2\_X1 g12747(.A1 (savings\_local[8]), .A2 (amount[8]), .ZN (n\_63));

OR2\_X1 g12791(.A1 (chequing\_local[12]), .A2 (amount[12]), .Z (n\_21));

NAND2\_X1 g12780(.A1 (savings\_local[12]), .A2 (amount[12]), .ZN

(n\_47));

NOR2\_X1 g12762(.A1 (savings\_local[6]), .A2 (amount[6]), .ZN (n\_74));

NOR2\_X1 g12796(.A1 (savings\_local[4]), .A2 (amount[4]), .ZN (n\_20));

NAND2\_X1 g12785(.A1 (chequing\_local[9]), .A2 (amount[9]), .ZN

(n\_123));

OR2\_X1 g12784(.A1 (chequing\_local[10]), .A2 (amount[10]), .Z (n\_19));

NAND2\_X1 g12773(.A1 (savings\_local[2]), .A2 (amount[2]), .ZN (n\_124));

NAND2\_X1 g12790(.A1 (chequing\_local[4]), .A2 (amount[4]), .ZN (n\_70));

NAND2\_X1 g12745(.A1 (chequing\_local[2]), .A2 (amount[2]), .ZN

(n\_115));

OR2\_X1 g12748(.A1 (chequing\_local[5]), .A2 (amount[5]), .Z (n\_18));

NOR2\_X1 g12750(.A1 (savings\_local[12]), .A2 (amount[12]), .ZN

(n\_125));

NOR2\_X1 g12770(.A1 (savings\_local[11]), .A2 (amount[11]), .ZN (n\_51));

NOR2\_X1 g12752(.A1 (savings\_local[2]), .A2 (amount[2]), .ZN (n\_61));

NOR2\_X1 g12758(.A1 (chequing\_local[11]), .A2 (amount[11]), .ZN

(n\_57));

NAND2\_X1 g12759(.A1 (savings\_local[6]), .A2 (amount[6]), .ZN (n\_114));

NOR2\_X1 g12795(.A1 (chequing\_local[9]), .A2 (amount[9]), .ZN (n\_76));

NAND2\_X1 g12768(.A1 (savings\_local[0]), .A2 (amount[0]), .ZN (n\_104));

NAND2\_X1 g12775(.A1 (chequing\_local[1]), .A2 (amount[1]), .ZN

(n\_117));

NOR2\_X1 g12786(.A1 (state[2]), .A2 (state[1]), .ZN (n\_188));

OR2\_X1 g12749(.A1 (chequing\_local[8]), .A2 (amount[8]), .Z (n\_17));

NAND2\_X1 g12756(.A1 (chequing\_local[6]), .A2 (amount[6]), .ZN

(n\_116));

NOR2\_X1 g12754(.A1 (chequing\_local[1]), .A2 (amount[1]), .ZN (n\_59));

NOR2\_X1 g12849(.A1 (state[3]), .A2 (rst), .ZN (n\_16));

NOR2\_X1 g12798(.A1 (savings\_local[9]), .A2 (amount[9]), .ZN (n\_121));

NAND2\_X1 g12744(.A1 (savings\_local[11]), .A2 (amount[11]), .ZN

(n\_126));

OR2\_X1 g12776(.A1 (savings\_local[5]), .A2 (amount[5]), .Z (n\_15));

NOR2\_X1 g12787(.A1 (chequing\_local[4]), .A2 (amount[4]), .ZN (n\_119));

NOR2\_X1 g12760(.A1 (pin[9]), .A2 (pin[8]), .ZN (n\_14));

NOR2\_X1 g12767(.A1 (chequing\_local[2]), .A2 (amount[2]), .ZN (n\_53));

NAND2\_X1 g12764(.A1 (savings\_local[9]), .A2 (amount[9]), .ZN (n\_55));

NOR2\_X1 g12772(.A1 (savings\_local[7]), .A2 (amount[7]), .ZN (n\_49));

NAND2\_X1 g12777(.A1 (chequing\_local[0]), .A2 (amount[0]), .ZN

(n\_129));

INV\_X1 g12867(.I (savings\_local[12]), .ZN (n\_313));

INV\_X1 g12885(.I (amount[4]), .ZN (n\_202));

INV\_X1 g12883(.I (amount[7]), .ZN (n\_68));

INV\_X1 g12886(.I (amount[11]), .ZN (n\_301));

INV\_X1 g12859(.I (state[2]), .ZN (n\_65));

INV\_X1 g12873(.I (chequing\_local[11]), .ZN (n\_13));

INV\_X1 g12852(.I (savings\_local[6]), .ZN (n\_12));

INV\_X1 g12892(.I (amount[9]), .ZN (n\_278));

INV\_X1 g12855(.I (savings\_local[2]), .ZN (n\_32));

INV\_X1 g12857(.I (savings\_local[8]), .ZN (n\_11));

INV\_X1 g12862(.I (chequing\_local[6]), .ZN (n\_10));

INV\_X1 g12884(.I (amount[6]), .ZN (n\_230));

INV\_X1 g12879(.I (amount[2]), .ZN (n\_180));

INV\_X1 g12890(.I (amount[3]), .ZN (n\_31));

INV\_X1 g12868(.I (savings\_local[11]), .ZN (n\_41));

INV\_X1 g12860(.I (chequing\_local[2]), .ZN (n\_9));

INV\_X1 g12858(.I (chequing\_local[1]), .ZN (n\_8));

INV\_X1 g12887(.I (deposit\_withdrawal\_selection), .ZN (n\_7));

INV\_X1 g12853(.I (state[0]), .ZN (n\_332));

INV\_X1 g12893(.I (amount[12]), .ZN (n\_26));

INV\_X1 g12891(.I (amount[10]), .ZN (n\_69));

INV\_X1 g12889(.I (amount[13]), .ZN (n\_322));

INV\_X1 g12874(.I (amount[8]), .ZN (n\_39));

INV\_X1 g12869(.I (savings\_local[10]), .ZN (n\_44));

INV\_X1 g12854(.I (state[3]), .ZN (n\_150));

INV\_X1 g12856(.I (chequing\_local[9]), .ZN (n\_6));

INV\_X1 g12882(.I (rst), .ZN (n\_425));

INV\_X1 g12863(.I (chequing\_local[7]), .ZN (n\_5));

INV\_X1 g12877(.I (pin[0]), .ZN (n\_4));

INV\_X1 g12870(.I (chequing\_local[4]), .ZN (n\_3));

INV\_X1 g12865(.I (savings\_local[9]), .ZN (n\_2));

INV\_X1 g12888(.I (pin[10]), .ZN (n\_1));

INV\_X1 g12875(.I (pin[4]), .ZN (n\_0));

INV\_X1 g12876(.I (amount[1]), .ZN (n\_46));

INV\_X1 g12864(.I (savings\_local[7]), .ZN (n\_28));

INV\_X1 g12881(.I (amount[5]), .ZN (n\_72));

INV\_X1 g12878(.I (account\_selection), .ZN (n\_324));

INV\_X1 g12880(.I (amount[0]), .ZN (n\_67));

INV\_X1 g12866(.I (savings\_local[4]), .ZN (n\_204));

INV\_X1 g12871(.I (state[1]), .ZN (n\_40));

INV\_X1 g12861(.I (savings\_local[13]), .ZN (n\_98));

INV\_X1 g12872(.I (savings\_local[1]), .ZN (n\_105));

endmodule